ADVANCES IN DESIGN AND SPECIFICATION LANGUAGES FOR SOCS pdf

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*Advances in Design and Specification Languages for SoCs: Selected Contributions from FDL'04 [Pierre Boulet] on www.enganchecubano.com *FREE* shipping on qualifying offers. This book is the sixth in the ChDL (Chip Design Languages) series.*

Output of PWM driver with different sample frequencies. Discussion SystemC provides a very generic approach for modeling digital systems. However, all models of computation are simulated by a discrete event simulator. Models of computation that have different interfaces or value types can only be converted, if they are subtypes. However, modeling of mixed-signal systems at block diagram level negotiates many problems that occur in analog circuit design, and that have impact on system behavior. Mixed-Signal Extension for SystemC. Kluwer Academic Publishers, Apr In SystemC â€" Methodologies and Applications. Christoph Grimm and Klaus Waldschmidt. Repartitioning and technologymapping of electronic hybrid systems. Journal of Circuits, Systems, and Computers, June Edward Lee and Yuhong Xiong. A Behavioral type system and its application in Ptolemy II. Formal Aspects of Computing, Technical report, Open SystemC Initiative, A mixed net arises in mixed-signal design as the result of interconnecting components modeled in different domains, in particular when connecting a discrete and a continuous port. Hardware description languages do not support such connections directly. They require the insertion of an appropriate conversion model between the dissimilar ports. Using conversion models correctly, a mixed net can be successfully partitioned and modeled with the desired blend of accuracy and performance. Conversion models are explained, including criteria for what makes a good one. Strategies for partitioning a mixed net and inserting conversion models are discussed. Printed in the Netherlands. Introduction Our goal is to describe and simulate a mixed-signal system design with the required accuracy. But in order to verify some aspects, the most complex implementation models are needed. The design process using VHDLAMS still leads to structural problems when switching between two models designed to represent the same component in different domains. In an electrical system, for example, the discrete domain is modeled by concurrently executing processes that communicate through signals of some logic type like std logic. The electrical nature in the continuous domain is modeled with differentialalgebraic equations of voltages, currents, and other unknowns. These models may be conservative systems, i. A complete set of electrical components that can be used together for modeling a mixed-signal system will include digital models and both types of analog models. One component may have a set of models in different domains designed to be equivalent. Models that are from different domains have both different implementations and interfaces. Nevertheless, the interfaces are closely related. There is an equivalence between corresponding ports, i. Any component from the mixed-signal set may be connected to others to form a system model. It turns out that suitable domain conversions must be designed as models themselves and be part of the component set. Effective system design styles can be supported if it is possible to specify reasonable rules to insert conversion models automatically and to bind implementations of such models to each instance of a conversion model. Nevertheless, portions may be written directly in the HDL or generated from other design tools. A top-down design methodology leads from a high level of design abstraction at the system or behavioral level to a lower level of abstraction going toward the physical implementation level. Moving top-down in abstraction does not necessarily mean crossing modeling domain. Some components may move from behavioral to rtl to gate level to switch level and remain discrete models. If one can safely avoid using the circuit level model in the system model, the designer asserts that the digital model is equivalent to its analog counterpart. There are few straightforward paths in top-down design for mixed-signal systems. Analog subsystems have comparatively little synthesis. If your mixedsignal component set has analog components with a high level behavioral model and low level implementation model, it supports both top-down and bottom-up modeling. Designing an analog model may start with circuit topology at the implementation level and be modeled upwards, or from a top-down behavioral model and be modeled downwards. If you require an equivalent model at another abstraction level, there are two cases to consider. From the implementation model, there is a more organized and potentially automated transition upwards to the behavioral model. Back at the system level, it may be ideal to simulate the entire system at the analog implementation level. Schematic entry systems are effective, in part. Unfortunately, they are not usable where component interfaces change across domains. After reviewing the mixed net modeling and conversion concepts, a solution to this problem will be proposed. Mixed Nets and Conversion Models A net consists of a root, typically a terminal, quantity or signal declared in a block, and all ports connected to the root, including transitive connections. Its structure is a tree. A mixed net is a net whose root and connected ports belong to different object classes. In a typical mixed net, some leaves of the tree may be terminal ports, other leaves may be quantity ports, and still others may be signal ports. Nonetheless, these ports and the root must be declared to be objects of a particular class: Other AMS languages have similar uniformity rules for nets. Therefore, to perform a simulation, a mixed net must be split into uniform portions using some partitioning strategy, and suitable code must be inserted at the boundaries of the different portions of the net to convert between the semantics of, for example, a terminal and a signal. The preferable way to manage such conversion code is to place it in conversion models, which then are instantiated such that they link the different portions of the net. The object classes represent different modeling domains. Instances of conversion models are inserted between the formal and the actual of a port association element if the formal and actual are of different object classes. For example, it is easily possible that a mixed net might have several disjoint terminal nets or nodes , each with a different potential. The remaining three strategies have two aspects in common: We ignore the object class of the root and the intermediate ports and only honor the object class of the ports that are leaves of the tree forming the net. We also consider the object classes to correspond to abstraction levels, with a terminal being the most detailed and a signal being the most abstract. Partitioning Driven by Elaboration. This strategy considers, for each vertex in the tree describing the net, the object class of the vertex and its immediate children and converts this portion of the net to the most detailed of these object classes. If the result is different from the object class of the vertex, then an instance of a conversion model is inserted between the vertex and its ancestor. Its drawback is the sensitivity of its result to changes of a leaf port: That is, a structural design change may lead to an unexpected change in the mixed net representation and surprising behaviour. The goal of this strategy is to minimize the number of instances of conversion models. The advantage of this strategy is performance. In this strategy, a mixed net is converted in its entirety to a uniform net whose object class is that of the most detailed object class of the root or any port of the net. For example, if any terminal is connected to the net, then the net is converted to a terminal. Instances of conversion models are inserted between the net and any leaf port whose object class is different from the object class of the net. Its drawback is the potentially large number of instances of conversion models, and performance may be affected by the models of the lowest abstraction connected to the net as well as by the number of conversion model instances 2. To also satisfy the VHDL-AMS rules about port association elements, which are based on the mode of the formal port, we end up with seven categories of conversion models: Mixed Nets, Conversion Models, and VHDL-AMS 27 It is apparent from this list that a conversion model always has a direction, even in the case of a bidirectional conversion model, where the direction changes over time, driven either by the operation of the conversion model or by control information such as switching on the signal end of the conversion model between high impedance input and driving output state. Each category of conversion models is further parameterized by the type of the signal or quantity or the nature of the terminal on either end of the conversion model. Regardless of the partitioning strategy, any mechanism to bind a category of conversion models to a particular implementation of a conversion model must be rich enough to support this parameterization. For an input or output object of class terminal, this includes the possibility of converting between its reference quantity for an electrical terminal: Conversion models between terminals and quantities are straightforward to implement because of the closeness of the semantics of the two object classes. A TQ conversion model is essentially a quantity source whose value is controlled by the reference or contribution quantity of the terminal. Similarly, a QT conversion model is either a quantity controlled across source or a quantity controlled through source. Conversion models between signals and quantities or terminals have some similarities in that they involve converting between discrete time semantics and continuous time semantics. For a d2a or an SQ conversion model, the general approach is that of a controlled source whose value is driven by the value of the signal. A bidirectional conversion model combines the functionality of an a2d and a d2a conversion model, possibly with some extra code to switch its direction. In the remainder of this section, we will focus on a2d and d2a conversion models; SQ and QS conversion models are essentially subsets of a2d and d2a. We further restrict the discussion to conversion models with an electrical terminal and a signal of type std logic. In either case, the conversion model can be parameterized to match the properties of a particular physical device. Ideal conversion models are the easiest to implement. As examples, we show the implementation of ideal a2d and d2a conversion models converting to or from a voltage. A possible implementation of the model and the corresponding FSM are shown in Figure 2. The corresponding ideal d2a conversion model can be implemented as a voltage source with an output resistance where both the output voltage and the resistance are controlled by the signal value. A possible implementation of the model is shown in Figure 2. For example, the driving characteristics of a conversion model for the cmos technology can be modeled by describing the channel properties of the two transistors at the output of a cmos gate, with its operation controlled by the input signal value. Conversion models with such detail typically need additional ports that provide the power supply for the model and the reference. Current Approaches to Automatic Insertion of Conversion Models Once appropriate conversion models have been designed and components that give rise to their use are available, the designer focuses on the system design task. The designer is engaged in structural composition tasks, and automatic insertion of conversion models is very desirable for improved productivity, repeatability, and correctness.

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