# DIGITAL LOGIC DESIGN VIVA QUESTIONS AND ANSWERS pdf

## 1: + TOP DIGITAL ELECTRONICS Questions and Answers Pdf DIGITAL ELECTRONICS Questions

*Digital Logic Design VIVA Questions and Answers: 1) Explain about setup time and hold time, what will happen if there is setup time and hold tine Skip to content Engineering interview questions,Mcqs,Objective Questions,Class Notes,Seminor topics,Lab Viva Pdf free download.*

In Boolean algebra, the true state is denoted by the number one, referred as logic one or logic high. While, the false state is represented by the number zero, called logic zero or logic low. And in the digital electronic, the logic high is denoted by the presence of a voltage potential. It has one out input and one output. It has one output due to the combination of two output. Either of the value will show the same output. Binary number consists of either 0 or 1, in simple words number 1 represents the ON state and number 0 represents OFF state. These binary numbers can combine billion of machines into one machines or circuit and operate those machines by performing arithmetic calculations and sorting operations. It uses two Bi-polar Junction Transistors in the design of each logic gate TTL chips can consist of a substantial number of parts like resistors TTLS chip consumes lot more power especially at rest. It is also an integrated chip but used field effect transistors in the design CMOS has greater density for logic gates. A sequential circuit is a circuit which is created by logic gates such that the required logic at the output depends not only on the current input logic conditions, but also on the sequences past inputs and outputs. Verilog can be different to normal programming language in following aspects Simulation time concept Basic circuit concepts like primitive gates and network connections 7 Explain what is Verilog? In Verilog, circuit components are prepared inside a Module. It contains both behavioral and structural statements. Structural statements signify circuit components like logic gates, counters and micro-processors. Behavioral statements represent programming aspects like loops, if-then statements and stimulus vectors. The two types of procedural blocks in Verilog are Initial: Initial blocks runs only once at time zero Always: MOSFET has three regions of operations Cut-off region Triode region Saturation region The triode and cut-off region are used to function as a switch, while, saturation region is used to operate as an amplifier. When positive voltage is transmitted across Gate, it causes the free holes positive charge to be pushed back or repelled from the region of the substrate under the Gate. When these holes are pushed down the substrate, they leave behind a carrier depletion region. Higher the number of stacks, slower the gate will be. So input are restricted to four. A multiplexer is a combination circuit which selects one of the many input signals and direct to the only output. SCR is a 4 layered solid state device which controls current flow. It is a type of rectifier that is controlled by a logical gate signal. It is a 4 layered, 3-terminal device. Slack is referred as a time delay difference from the expected delay to the actual delay in a particular path. Slack can be negative or positive. With the keyword defparam, parameter values can be configured in any module instance in the design.

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## 2: Digital Electronics Questions and Answers

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Set up time is the amount of time before the clock edge that the input signal needs to be stable to guarantee it is accepted properly on the clock edge. Hold time is the amount of time after the clock edge that same input signal has to be held before changing it to make sure it is sensed properly at the clock edge. Whenever there are setup and hold time violations in any flip-flop, it enters a state where its output is unpredictable: This whole process is known as metastability 2 What is skew, what are problems associated with it and how to minimize it? In circuit design, clock skew is a phenomenon in synchronous circuits in which the clock signal sent from the clock circuit arrives at different components at different times. This is typically due to two causes. The first is a material flaw, which causes a signal to travel faster or slower than expected. The second is distance: Clock skew can cause harm in two ways. Suppose that a logic path travels through combinational logic from a source flip-flop to a destination flip-flop. If the destination flip-flop receives the clock tick later than the source flip-flop, and if the logic path delay is short enough, then the data signal might arrive at the destination flip-flop before the clock tick, destroying there the previous data that should have been clocked through. This is called a hold violation because the previous data is not held long enough at the destination flip-flop to be properly clocked through. If the destination flip-flop receives the clock tick earlier than the source flip-flop, then the data signal has that much less time to reach the destination flip-flop before the next clock tick. If it fails to do so, a setup violation occurs, so-called because the new data was not set up and stable before the next clock tick arrived. A hold violation is more serious than a setup violation because it cannot be fixed by increasing the clock period. Clock skew, if done right, can also benefit a circuit. The optimal set of clock delays is determined by a linear program, in which a setup and a hold constraint appears for each logic path. In this linear program, zero clock skew is merely a feasible point. Clock skew can be minimized by proper routing of clock signal clock distribution tree or putting variable delay buffer so that all clock inputs arrive at the same time 3 What is slack? What causes it explain with waveform? How to overcome it? The following figure shows a synchronous alternative to the gated clock using a data path. The flip-flop is clocked at every clock cycle and the data path is controlled by an enable. When the enable is Low, the multiplexer feeds the output of the register back on itself. When the enable is High, new data is fed to the flip-flop and the register changes its state 5 Given only two xor gates one must function as buffer and another as inverter? Tie one of xor gates input to 1 it will act as inverter. Tie one of xor gates input to 0 it will act as buffer. The main difference between latch and FF is that latches are level sensitive while FF are edge sensitive. They both require the use of clock signal and are used in sequential logic. For a latch, the output tracks the input when the clock signal is high, so as long as the clock is logic 1, the output can change if the input also changes. Difference between heap and stack? The Heap is more or less responsible for keeping track of our objects our data, well Think of the Stack as a series of boxes stacked one on top of the next. The Heap is similar except that its purpose is to hold information not keep track of execution most of the time so anything in our Heap can be accessed at any time. With the Heap, there are no constraints as to what can be accessed like in the stack. The Heap is like the heap of clean laundry on our bed that we have not taken the time to put away yet - we can grab what we need quickly. The Stack is like the stack of shoe boxes in the closet where we have to take off the top one to get to the one underneath it. A Mealy and Moore models are the basic models of state machines. A state machine which uses only Entry Actions, so that its output depends on the state, is called a Moore model. A state machine which uses only Input Actions, so that the output depends on the state and also on inputs, is called a Mealy model. The models selected will influence a design but there are no general indications as to which model is better. Choice of a model depends on the application, execution means for instance, hardware systems are usually best realized as Moore models and personal preferences of a designer or programmer B Mealy machine has outputs that depend on the state and input thus, the FSM has the output written on edges Moore machine has outputs that depend on state only thus, the FSM has the output written in

the state itself. Adv and Disadv In Mealy as the output variable is a function both input and state, changes of state of the state variables will be delayed with respect to changes of signal level in the input variables, there are possibilities of glitches appearing in the output variables. Moore overcomes glitches as output dependent on only states and not the input signal level. All of the concepts can be applied to Moore-model state machines because any Moore state machine can be implemented as a Mealy state machine, although the converse is not true. The outputs are held until you go to some other state Mealy machine: Mealy machines give you outputs instantly, that is immediately upon receiving input, but the output is not held after that clock cycle. Common classifications used to describe the state encoding of an FSM are Binary or highly encoded and One hot. A binary-encoded FSM design only requires as many flip-flops as are needed to uniquely encode the number of states in the state machine. The actual number of flip-flops required is equal to the ceiling of the log-base-2 of the number of states in the FSM. A onehot FSM design requires a flip-flop for each state in the design and only one flip-flop the flip-flop representing the current or "hot" state is set at a time in a one hot FSM design. For a state machine with 9- 16 states, a binary FSM only requires 4 flip-flops while a onehot FSM requires a flip-flop for each state in the design FPGA vendors frequently recommend using a onehot state encoding style because flip-flops are plentiful in an FPGA and the combinational logic required to implement a onehot FSM design is typically smaller than most binary encoding styles. You can find answer to this in timing. SDRAM receives its address command in two address words. It uses a multiplex scheme to save input pins. This is the basic question that many interviewers ask. It is well known that in left shift all bits will be shifted left and LSB will be appended with 0 and in right shift all bits will be shifted right and MSB will be appended with 0 this is a straightforward answer What is expected is in a left shift value gets Multiplied by 2 eg:

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## 3: Digital design interview questions & answers

*Digital logic circuits important question and answers for 5 units 1. 1 Digital Logic Circuits 2 marks1) Given the two binary numbers X = and Y = , perform the subtraction (a)X -Y and (b) Y - X using 2's complements.*

Digital electronics is also that branch of science that uses fibre optics to detect digital display. Most of the reputed electronics companies put up their questions from this portion of electronics. So to assist the aspirants, we are providing here some frequently asked interview questions and answers on digital electronics: Explain about setup time and hold time, what will happen if there is setup time and hold tine violation, how to overcome this? For Synchronous flip-flops, we have special requirements for the inputs with respect to clock signal input there are Setup Time: Minimum time Period during which data must be stable before the clock makes a valid transition. Minimum time period during which data must be stable after the clock has made a valid transition. R and S in the case of RS flip-flop should be stable for at least 1 ns after clock has made transition from 0 to 1 Hold time is the amount of time after the clock edge that same input signal has to be held before changing it to make sure it is sensed properly at the clock edge. Whenever there are setup and hold time violations in any flip-flop, it enters a state where its output is unpredictable: This whole process is known as metastability: What is difference between latch and flip-flop? The main difference between latch and FF is that latches are level sensitive while FF is edge sensitive. They both require the use of clock signal and are used in sequential logic. For a latch, the output tracks the input when the clock signal is high, so as long as the clock is logic 1, the output can change if the input also changes. FF on the other hand, will store the input only: Latch is sensitive to glitches on enable pin, whereas flip-flop is immune to glitches. Latches take fewer gates also less power to implement than flip-flops. Latches are faster than flip-flops. Ans Tie one of xor gates input to 1 it will act as inverter. Tie one of xor gates input to 0 it will act as buffer. Ques 4 Difference between Mealy and Moore state machine? Ans Mealy and Moore models are the basic models of state machines. A state machine which uses only Entry Actions, so that its output depends on the state, is called a Moore model. A state machine which uses only Input Actions, so that the output depends on the state and also on inputs, is called a Mealy model. Mealy machine has outputs that depend on the state and input thus, the FSM has the output written on edges Moore machine has outputs that depend on state only thus, the FSM has the output written in the state itself. In Mealy as the output variable is a function both input and state, changes of state of the state variables will be delayed with respect to changes of signal level in the input variables, there are possibilities of glitches appearing in the output variables. Moore overcomes glitches as output dependent on only states and not the input signal level. All of the concepts can be applied to Moore-model state machines because any Moore state machine can be implemented as: The outputs are held until you go to some other state Mealy machine: Mealy machines give you outputs instantly, that is immediately upon receiving input, but the output is not held after that clock cycle.: Common classifications used to describe the state encoding of an FSM are Binary or highly encoded and One hot. A binary-encoded FSM design only requires as many flip-flops as are needed to uniquely encode the number of states in the state machine. The actual number of flip-flops required is equal to the ceiling of the log-base-2 of the number of states in the FSM. For a state machine with 9- 16 states, a binary FSM only requires 4 flip-flops while a one hot FSM requires a flip-flop for each state in the design FPGA vendors frequently recommend using a one hot state encoding style because flip-flops are plentiful in an FPGA and the combinational logic required to implement a one hot FSM design is typically smaller than most binary encoding styles. Ques 6 How to achieve degree exact phase shift?: SDRAM receives its address command in two address words. It uses a multiplex scheme to save input pins. Ques 8 Tell some of applications of buffer? Why is most interrupts active low? This answers why most signals are active low if you consider the transistor level of a module, active low means the capacitor in the output terminal gets charged or discharged based on low to high and high to low transition respectively. When it goes from high to low it depends on the: Hence people prefer using active low signals.: We hope that the given set of questions and answers on digital electronics satisfies your needs and so we would like to have some feedback from your part so as to improve it. Please put your valuable feedback in the comment the box.: Share this on your

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## 4: Top 17 VLSI Interview Questions & Answers

*Digital Electronics questions and answers with explanation for interview, competitive examination and entrance test. Fully solved examples with detailed answer description, explanation are given and it would be easy to understand.*

A multiplexer is a combinational circuit which selects one of many input signals and directs to the only output. What is a ring counter? Answer A ring counter is a type of counter composed of a circular shift register. The output of the last shift register is fed to the input of the first register. For example, in a 4-register counter, with initial register values of , the repeating pattern is: Compare and Contrast Synchronous and Asynchronous reset. Answer Synchronous reset logic will synthesize to smaller flip-flops, particularly if the reset is gated with the logic generating the d-input. But in such a case, the combinational logic gate count grows, so the overall gate count savings may not be that significant. The clock works as a filter for small reset glitches; however, if these glitches occur near the active clock edge, the Flip-flop could go metastable. In some designs, the reset must be generated by a set of internal conditions. A synchronous reset is recommended for these types of designs because it will filter the logic equation glitches between clock. Problem with synchronous resets is that the synthesis tool cannot easily distinguish the reset signal from any other data signal. Synchronous resets may need a pulse stretcher to guarantee a reset pulse width wide enough to ensure reset is present during an active edge of the clock, if you have a gated clock to save power, the clock may be disabled coincident with the assertion of reset. Only an asynchronous reset will work in this situation, as the reset might be removed prior to the resumption of the clock. Designs that are pushing the limit for data path timing, can not afford to have added gates and additional net delays in the data path due to logic inserted to handle synchronous resets. The major problem with asynchronous resets is the reset release, also called reset removal. Using an asynchronous reset, the designer is guaranteed not to have the reset added to the data path. Another advantage favoring asynchronous resets is that the circuit can be reset with or without a clock present. Ensure that the release of the reset can occur within one clock period else if the release of the reset occurred on or near a clock edge then flip-flops may go into metastable state. What is a Johnson counter? Answer Johnson counter connects the complement of the output of the last shift register to its input and circulates a stream of ones followed by zeros around the ring. For example, in a 4-register counter, the repeating pattern is: An assembly line has 3 fail safe sensors and one emergency shutdown switch. The line should keep moving unless any of the following conditions arise: How many minimum number of 2 input NAND gates are required?

## 5: Digital Design Interview Questions - All in 1

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## 8: Multiple Choice Questions on Logic Gates - Examtime Quiz

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*Digital design interview questions & answers. 1) Explain about setup time and hold time, what will happen if there is setup time and hold tine violation, how to overcome this? Set up time is the amount of time before the clock edge that the input signal needs to be stable to guarantee it is accepted properly on the clock edge.*

## 9: Logic Gates - Digital Electronics Questions and Answers

*Designer must how data flows between various registers of the www.enganchecubano.com level: The module is implemented in terms of logic gates and interconnections between these gates. Designer should know the gate-level diagram of the www.enganchecubano.com level: This is the lowest level of abstraction.*

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