# HIGH PERFORMANCE CURRENT SCALING DIGITAL-TO-ANALOG CONVERTER DESIGN pdf

## 1: Analog-to-digital converter - Wikipedia

*This article will look at some of the most important features of the AD, a new ADC from Analog Devices that is intended for low-power data acquisition (DAQ) designs. The AD is a single-channel high-performance sigma-delta ADC which offers a programmable output data rate (ODR) up to*

Direct-conversion[ edit ] A direct-conversion ADC or flash ADC has a bank of comparators sampling the input signal in parallel, each firing for their decoded voltage range. The comparator bank feeds a logic circuit that generates a code for each voltage range. Direct conversion is very fast, capable of gigahertz sampling rates, but usually has only 8 bits of resolution or fewer, since the number of comparators needed, 2N â€" 1, doubles with each additional bit, requiring a large, expensive circuit. ADCs of this type have a large die size, a high input capacitance , high power dissipation, and are prone to produce glitches at the output by outputting an out-of-sequence code. Scaling to newer submicrometre technologies does not help as the device mismatch is the dominant design limitation. They are often used for video , wideband communications or other fast signals in optical storage. There are four different types of direct ADCs. It is at the same time the fastest and the most expensive technique. The circuit consists of a resistive divider network, a set of op-amp comparators and a priority encoder. A small amount of hysteresis is built into the comparator to resolve any problems that might occur if both inputs were of equal voltage. At each node of the resistive divider, a comparison voltage is available. The purpose of the circuit is to compare the analog input voltage with each of the node voltages. The circuit has the advantage of high speed as the conversion takes place simultaneously rather than sequentially. Typical conversion time is ns or less. Conversion time is limited only by the speed of the comparator and of the priority encoder. This type of ADC has the disadvantage that the number of comparators required almost doubles for each added bit. Also, the larger the value of n, the more complex is the priority encoder. The circuit consists of an up-down counter with the comparator controlling the direction of the count. The analog output of the DAC is compared with the analog input. If the input is greater than the DAC output signal, the output of the comparator goes high and the counter is caused to count up. The tracking ADC has an advantage of being simple. The disadvantage, however, is the time needed to stabilize as a new conversion value is directly proportional to the rate at which the analog signal changes. Successive approximation[ edit ] A successive-approximation ADC uses a comparator to successively narrow a range that contains the input voltage. At each successive step, the converter compares the input voltage to the output of an internal digital to analog converter which might represent the midpoint of a selected voltage range. At each step in this process, the approximation is stored in a successive approximation register SAR. For example, consider an input voltage of 6. For the first step, the input 6. For the second step, the input voltage is compared to 4 V midpoint of 0â€"8. The steps are continued until the desired resolution is reached. Ramp-compare[ edit ] A ramp-compare ADC produces a saw-tooth signal that ramps up or down then quickly returns to zero. When the ramp starts, a timer starts counting. Timed ramp converters require the fewest transistors. The ramp time is sensitive to temperature because the circuit generating the ramp is often a simple oscillator. There are two solutions: A special advantage of the ramp-compare system is that comparing a second signal just requires another comparator, and another register to store the voltage value. A very simple non-linear ramp-converter can be implemented with a microcontroller and one resistor and capacitor. This has the advantage that a slow comparator cannot be disturbed by fast input changes. The Wilkinson ADC is based on the comparison of an input voltage with that produced by a charging capacitor. The capacitor is allowed to charge until its voltage is equal to the amplitude of the input pulse a comparator determines when this condition has been reached. Then, the capacitor is allowed to discharge linearly, which produces a ramp voltage. At the point when the capacitor begins to discharge, a gate pulse is initiated. The gate pulse remains on until the capacitor is completely discharged. Thus the duration of the gate pulse is directly proportional to the amplitude of the input pulse. This gate pulse operates a linear gate which receives pulses from a high-frequency oscillator clock. While the gate

is open, a discrete number of clock pulses pass through the linear gate and are counted by the address register. The time the linear gate is open is proportional to the amplitude of the input pulse, thus the number of clock pulses recorded in the address register is proportional also. Alternatively, the charging of the capacitor could be monitored, rather than the discharge. Then a known reference voltage of opposite polarity is applied to the integrator and is allowed to ramp until the integrator output returns to zero the run-down period. The input voltage is computed as a function of the reference voltage, the constant run-up time period, and the measured run-down time period. Likewise, the speed of the converter can be improved by sacrificing resolution. Converters of this type or variations on the concept are used in most digital voltmeters for their linearity and flexibility. Charge balancing ADC The principle of charge balancing ADC is to first convert the input signal to a frequency using a voltage to frequency converter. This frequency is then measured by a counter and converted to an output code proportional to the analog input. The main advantage of these converters is that it is possible to transmit frequency even in noisy environment or in isolated form. Dual-slope ADC The analog part of the circuit consists of a high input impedance buffer,precision integrator and a voltage comparator. The converter first integrates the analog input signal for a fixed duration and then it integrates an internal reference voltage of opposite polarity until the integrator output is zero. The main disadvantage of this circuit is the long duration time. They are particularly suitable for accurate measurement of slowly varying signals such as thermocouples and weighing scales. The input signal and the DAC both go to a comparator. The comparator controls the counter. The number is read from the counter. Delta converters have very wide ranges and high resolution, but the conversion time is dependent on the input signal level, though it will always have a guaranteed worst-case. Delta converters are often very good choices to read real-world signals. Most signals from physical systems do not change abruptly. Some converters combine the delta and successive approximation approaches; this works especially well when high frequencies are known to be small in magnitude. Pipelined[ edit ] A pipelined ADC also called subranging quantizer uses two or more steps of subranging. First, a coarse conversion is done. In a second step, the difference to the input signal is determined with a digital to analog converter DAC. This difference is then converted finer, and the results are combined in a last step. This can be considered a refinement of the successive-approximation ADC wherein the feedback reference signal consists of the interim conversion of a whole range of bits for example, four bits rather than just the next-most-significant bit. By combining the merits of the successive approximation and flash ADCs this type is fast, has a high resolution, and only requires a small die size. Sigma-delta[ edit ] A sigma-delta ADC also known as a delta-sigma ADC oversamples the desired signal by a large factor and filters the desired signal band. Generally, a smaller number of bits than required are converted using a Flash ADC after the filter. The resulting signal, along with the error generated by the discrete levels of the Flash, is fed back and subtracted from the input to the filter. This negative feedback has the effect of noise shaping the error due to the Flash so that it does not appear in the desired signal frequencies. A digital filter decimation filter follows the ADC which reduces the sampling rate, filters off unwanted noise signal and increases the resolution of the output sigma-delta modulation , also called delta-sigma modulation. The result is that the sample rate is increased M times compared to what each individual ADC can manage. Intermediate FM stage[ edit ] An ADC with intermediate FM stage first uses a voltage-to-frequency converter to convert the desired signal into an oscillating signal with a frequency proportional to the voltage of the desired signal, and then uses a frequency counter to convert that frequency into a digital count proportional to the desired signal voltage. Longer integration times allow for higher resolutions. The two parts of the ADC may be widely separated, with the frequency signal passed through an opto-isolator or transmitted wirelessly. Some such ADCs use sine wave or square wave frequency modulation ; others use pulse-frequency modulation. Such ADCs were once the most popular way to show a digital display of the status of a remote analog sensor. A time-stretch analog-to-digital converter TS-ADC digitizes a very wide bandwidth analog signal, that cannot be digitized by a conventional electronic ADC, by time-stretching the signal prior to digitization. It commonly uses a photonic preprocessor frontend to time-stretch the signal, which effectively slows the signal down in time and

compresses its bandwidth. As a result, an electronic backend ADC, that would have been too slow to capture the original signal, can now capture this slowed down signal. For continuous capture of the signal, the frontend also divides the signal into multiple segments in addition to time-stretching. Each segment is individually digitized by a separate electronic ADC. Finally, a digital signal processor rearranges the samples and removes any distortions added by the frontend to yield the binary data that is the digital representation of the original analog signal. This section does not cite any sources. Please help improve this section by adding citations to reliable sources. Unsourced material may be challenged and removed. July Learn how and when to remove this template message Commercial ADCs are usually implemented as integrated circuits. Most converters sample with 6 to 24 bits of resolution, and produce fewer than 1 megasample per second. Thermal noise generated by passive components such as resistors masks the measurement when higher resolution is desired. As of February , Mega- and giga-sample per second converters are available. Mega-sample converters are required in digital video cameras , video capture cards , and TV tuner cards to convert full-speed analog video to digital video files. Commercial ADCs often have several inputs that feed the same converter, usually through an analog multiplexer. Different models of ADC may include sample and hold circuits, instrumentation amplifiers or differential inputs, where the quantity measured is the difference between two voltages. Music recording[ edit ] Analog-to-digital converters are integral to s era music reproduction technology and digital audio workstation -based sound recording.

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## 2: AD Datasheet and Product Info | Analog Devices

*Cong, Yonghua, "Design techniques for high-performance current-steering digital-to-analog converters " ().Retrospective Theses and Dissertations.*

The model number is a specific version of a generic that can be purchased or sampled. Status Status indicates the current lifecycle of the product. This can be one of 4 stages: The model has not been released to general production, but samples may be available. The model is currently being produced, and generally available for purchase and sampling. The model has been scheduled for obsolescence, but may still be purchased for a limited time. The specific part is obsolete and no longer available. Other models listed in the table may still be available if they have a status that is not obsolete. Package Description The package for this IC i. An Evaluation Board is a board engineered to show the performance of the model, the part is included on the board. For detailed drawings and chemical composition please consult our Package Site. Pin Count Pin Count is the number of pins, balls, or pads on the device. Temperature Range This is the acceptable operating range of the device. The various ranges specified are as follows: Temperature ranges may vary by model. Please consult the datasheet for more information. International prices may differ due to local duties, taxes, fees and exchange rates. For volume-specific price or delivery quotes, please contact your local Analog Devices, Inc. Pricing displayed for Evaluation Boards and Kits is based on 1-piece pricing. Most orders ship within 48 hours of this date. Once an order has been placed, Analog Devices, Inc. It is important to note the scheduled dock date on the order entry screen. We do take orders for items that are not in stock, so delivery may be scheduled at a future date. Also, please note the warehouse location for the product ordered. Transit times from these sites may vary. Sample availability may be better than production availability. Please enter samples into your cart to check sample availability. For more information about lead-free parts, please consult our Pb Lead free information page. Select the purchase button to display inventory availability and online purchase options. The Sample button will be displayed if a model is available for web samples. If a model is not available for web samples, look for notes on the product page that indicate how to request samples or Contact ADI. Evaluation Boards Pricing displayed is based on 1-piece. Back Select a country Check Inventory Pricing displayed is based on 1-piece. International prices may vary due to local duties, taxes, fees and exchange rates. Save to myAnalog Sign in to myAnalog Region.

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## 3: Digital-to-analog converter - Wikipedia

*Digital to Analog Converters ICs Solutions Bulletin Design Resources ADI has always placed the highest emphasis on delivering products that meet the maximum levels of quality and reliability.*

Overview[ edit ] Ideally sampled signal. Piecewise constant output of a conventional DAC lacking a reconstruction filter. In a practical DAC, a filter or the finite bandwidth of the device smooths out the step response into a continuous curve. A DAC converts an abstract finite-precision number usually a fixed-point binary number into a physical quantity e. In particular, DACs are often used to convert finite-precision time series data to a continually varying physical signal. An ideal DAC converts the abstract numbers into a conceptual sequence of impulses that are then processed by a reconstruction filter using some form of interpolation to fill in data between the impulses. A conventional practical DAC converts the numbers into a piecewise constant function made up of a sequence of rectangular functions that is modeled with the zero-order hold. Other DAC methods such as those based on delta-sigma modulation produce a pulse-density modulated output that can be similarly filtered to produce a smoothly varying signal. As per the Nyquistâ€"Shannon sampling theorem , a DAC can reconstruct the original signal from the sampled data provided that its bandwidth meets certain requirements e. Digital sampling introduces quantization error that manifests as low-level noise in the reconstructed signal. To illustrate, consider a typical long-distance telephone call. The digital stream is then divided into network packets where it may be sent along with other digital data , not necessarily audio. The packets are then received at the destination, but each packet may take a completely different route and may not even arrive at the destination in the correct time order. The digital voice data is then extracted from the packets and assembled into a digital data stream. A DAC converts this back into an analog electrical signal, which drives an audio amplifier , which in turn drives a loudspeaker , which finally produces sound. Audio[ edit ] Most modern audio signals are stored in digital form for example MP3s and CDs and, in order to be heard through speakers, they must be converted into an analog signal. Specialist standalone DACs can also be found in high-end hi-fi systems. These normally take the digital output of a compatible CD player or dedicated transport which is basically a CD player with no internal DAC and convert the signal into an analog line-level output that can then be fed into an amplifier to drive speakers. Similar digital-to-analog converters can be found in digital speakers such as USB speakers, and in sound cards. Top-loading CD player and external digital-to-analog converter. Given this inherent distortion, it is not unusual for a television or video projector to truthfully claim a linear contrast ratio difference between darkest and brightest output levels of  Video signals from a digital source, such as a computer, must be converted to analog form if they are to be displayed on an analog monitor. A device that is distantly related to the DAC is the digitally controlled potentiometer , used to control an analog signal digitally. Play media IBM Selectric typewriter uses a mechanical digital-to-analog converter to control its typeball. A one-bit mechanical actuator assumes two positions: The motion of several one-bit actuators can be combined and weighted with a whiffletree mechanism to produce finer steps. The IBM Selectric typewriter uses such a system. This technique is often used for electric motor speed control and other applications. The oversampling technique allows for the use of a lower resolution DAC internally. A simple 1-bit DAC is often chosen because the oversampled result is inherently linear. The DAC is driven with a pulse-density modulated signal, created with the use of a low-pass filter , step nonlinearity the actual 1-bit DAC , and negative feedback loop, in a technique called delta-sigma modulation. This results in an effective high-pass filter acting on the quantization noise , thus steering this noise out of the low frequencies of interest into the megahertz frequencies of little interest, in a process called noise shaping. The quantization noise at these high frequencies is removed or greatly attenuated by use of an analog low-pass filter at the output sometimes a simple RC low-pass circuit is sufficient. Most very high resolution DACs greater than 16 bits are of this type due to its high linearity and low cost. Higher oversampling rates can relax the specifications of the output low-pass filter and enable

further suppression of quantization noise. A single integrator is a low-pass filter with a frequency response inversely proportional to frequency and using one such integrator in the noise-shaping loop is a first order delta-sigma modulator. Multiple higher order topologies such as MASH are used to achieve higher degrees of noise-shaping with a stable topology. The binary-weighted DAC, which contains individual electrical components for each bit of the DAC connected to a summing point. This summing point can a summing op-amp. Each input resistor in the summing op-amp would have values powers of two with most current at MSB since they have the same resistor voltage source. This is one of the fastest conversion methods but suffers from poor accuracy because of the high precision required for each individual voltage or current. Such high-precision components are expensive, so this type of converter is usually limited to 8-bit resolution or less. Individual resistors are enabled or bypassed in the network based on the digital input. Switched current source DAC, from which different current sources are selected based on the digital input. Switched capacitor DAC contains a parallel capacitor network. Individual capacitors are connected or disconnected with switches based on the input. This improves the precision due to the relative ease of producing equal valued-matched resistors or current sources. Individual bits of the digital input are processed each cycle until the entire input is accounted for. The thermometer-coded DAC, which contains an equal resistor or current-source segment for each possible value of DAC output. This is perhaps the fastest and highest precision DAC architecture but at the expense of high cost. Hybrid DACs, which use a combination of the above techniques in a single converter. Most DAC integrated circuits are of this type due to the difficulty of getting low cost, high speed and high precision in one device. The segmented DAC, which combines the thermometer-coded principle for the most significant bits and the binary-weighted principle for the least significant bits. In this way, a compromise is obtained between precision by the use of the thermometer-coded principle and number of resistors or current sources by the use of the binary-weighted principle. Most DACs, shown earlier in this list, rely on a constant reference voltage to create their output value. Alternatively, a multiplying DAC [5] takes a variable input voltage for their conversion. This puts additional design constraints on the bandwidth of the conversion circuit. Performance[ edit ] DACs are very important to system performance. The most important characteristics of these devices are: This is usually stated as the number of bits it uses, which is the base two logarithm of the number of levels. Resolution is related to the effective number of bits which is a measurement of the actual resolution attained by the DAC. Resolution determines color depth in video applications and audio bit depth in audio applications.

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