INTEGRATED FUNCTIONAL BLOCKS pdf

1: Function model - Wikipedia

Principles of integrated-circuit technology are considered along with elements of integrated functional blocks, models of transistors and diodes for integrated functional blocks, principles of.

An Integrated Programming technology is developed to program all the different controllers on the COB with one single program. This application is also a continuation in part CIP application of nonprovisional application Ser. In an embodiment, a function block integrated circuit directs the function of the system in response to the specific value of an external resistor detected. Other application specific functional circuits such as resistor identification circuits are provided outside the integrated circuit making use of discrete digital, analog components, or additional special function IC such as operational amplifiers and comparators. Since application circuit requirements vary, manufacturers are required to provide a family of micro-controllers IC each having a different functional, performance, or interfacing specifications to meet the different application needs of the users. This design of the IC is configured to provide a selected combination of the following preferred characteristics: Each audio or visual responses is predefined by one specific value of the identity passive component detected; 2. The sensing circuit should be able to detect a wide range of identity components, precisely responding to at least 20 to different values of the identity components; 4. Preferably only two input pins are required for the IC to detect the identity component; 5. The integrated circuit, including the precision detection circuit, should work with a voltage range representing the working conditions of two to three batteries. Acknowledging the variation of batteries under different loading conditions, the working voltage range is desirable for working in the voltage range of 2. The integrated circuit should not require external operational amplifier or comparator IC; 7. The standby current of the IC should be of a low value enabling the circuit to be always powered on for awaiting the contact of the identity passive component, a target standby current is below 10 uA; and 8. The circuit should be automatically switched from the microampere low current mode into the higher current working mode when an identity component touches the designated detection input pins. In a first application example of this IC, a doll having a voice generating chip is provided with two conductive contacts located at the lips of the doll. Food articles of different colors or shapes are provided with the play set. Each food article is provided internally a specific valued resistor connected to two conductive contacts exposed on the surface of the food article. When the doll is fed with a selected food article, the conductive contacts of the doll are connected with the internal resistor of the food article. The detection circuit inside the IC directs the voice generation circuit to produce a different food specific voice message in accordance to the identity of resistance value detected. Enlisted below are the standard commercial resistor values: Ohm range discarding resistance value below ohm: The k-ohm range is obtained by multiplying the above resistance values by 10 to provide another 24 different resistor values. The 10 k-ohm range is obtained by multiplying the above range of resistor values by to provide 24 additional resistor values. The k-ohm range resistor values is again obtained by multiplying the above resistor values by to provide further 24 resistor values. It means the high precision circuit provided by the subject invention is able to identify 97 different identity articles making use of a single commercial standard resistor in each article. It should be noted that among the 97 resistor values identified, some of the resistor values are less popular and can be considered as a secondary standard resistor value. Examples of these values are ohm, and ohm. Another challenge of the invention step is to provide a very low standby current, preferably to be lower than 10 uA; while still be able to initiate the detection circuit when a resistor is connected to the detection circuit input terminal. This requirement rules out the use of commercial analog comparators or operational amplifiers, as the standby current of these components is well above the desirable limit suitable for battery operation. Another difficulty of the input circuit design is for it to sense a broad range of resistance value, from ohm to 1M ohm, and initiate the IC from the low current standby mode to start performing the resistance detection process. In order to minimize the cost of the IC chip, the number of pins required by the resistor connection terminal is preferably to be limited to two pins as compare with three to four pins for lower resolution dual resistors detection circuit. In a first embodiment, a group of N or P channel MOS gates, each

can be switched on and off, provides a different reference resistance to the detection circuit for checking the external resistor value. The reference resistance is arranged to form a potential divider with the external resistor to trigger a voltage comparison circuit or an internal threshold switching circuit. In an alternate embodiment, the switched reference resistance can be used to control the current flowing through the external resistor for creating a reference voltage drop across the external resistor. Theoretically this voltage is proportional to the value of the external resistance and therefore it can be used to indirectly identify the external resistor. The detecting process requires a micro-controller programmed to properly switch the group of NMOS or PMOS gates, according to a predefined detection algorithm. Each of these gates represents a resistance value. Due to the tight resistor tolerance and the lax voltage supply requirements, an external reference component, preferably another low cost resistor is added to calibrate the circuit during the resistance identifying process. The reference component helps to compensate errors due to fabrication process of the IC, variation of the battery voltage and variation of logic transition threshold level inside the IC. It should be noted that the resistance ratio of a potential divider circuit is relatively independent of power supply voltage variation. Once an external resistor is identified by the detecting circuit, the controller directs an output response in accordance to the resistance value detected. Typical output responses including generating of different voice messages, starting or stopping a motor or to turn on and off an LED. In order to eliminate the requirement of an operational amplifier, the logic transition threshold of an IC can be used to detect the reference voltage created by an external resistor. Technically the sensitivity of an IC logic level transition switching threshold circuit is incomparable with that of an operational amplifier or a voltage comparator. In order to improve the detection sensitivity, an external transistor is included to amplifier the sensing current feeding to the input detection circuit. Alternately, the transistor can be reconfigured to form a switching circuit, which creates an external threshold switching sensor, that eliminates the variation caused by the fabrication process of the IC. To further improve the sensitivity, two external transistors are configured in the form of a Darlington pair to further increasing the current gain of a single transistor. It should be noted that the external bipolar transistors are not suitable to be integrated into the IC when it is fabricated with CMOS technology. When the resistance identification circuit is used to trigger different voice messages, the IC is required to provide a memory location to store compressed digital information representing the predefined messages. Existing commercially available voice generation chips are provided with different memory sizes to optimize the cost of voice chip for use in different applications that require different total voice durations. For example, each IC body of a typical voice generation IC product line may comprise a standard decoding circuit, a Digital to Analog conversion circuit and a speaker driver circuit, but a choice of different ROM sizes to provide 3 seconds, 6 seconds and up to multiple minutes for voice storage. Each of these IC members of the product line, although using substantially the same decoding circuit, requires a separated set of mask to build the IC. Accordingly the cost to develop the IC product line is proportional to the number of IC members designated in the product line according to the marketing requirement. Assuming a voice IC product line has ten different members, each providing a different total voice duration; by introducing an integrated resistor identity detection circuit, the product line is required to be expanded to 20 different IC members, ten with resistor identification capability and ten without. On the other hand, different IC applications require different number of IO input and output pads. Applications involving high number of keypads and an array of light indicators such as a child size follow me learning piano requires substantially more IO pads than a push a button, get a sound kind of simple toy. The number of IO pads forms a significant portion of the cost of an IC especially when the dice size of the IC is small. Accordingly in addition to the variation of memory size, different IC members may be included in the product line to tailor for different IO pads requirements. When the optional resistor directive feature is added, the number of possible combinations is extended to that is well beyond the reasonable number of IC members to be included in an IC product line. Each of these circuits may not be optimally fabricated by the same kind of technology. For example, most logic circuit is desirable to use CMOS technology; power circuit is more suitable to be fabricated by traditional power MOS technology or bipolar technology. RF circuit may require a further different technology. In order to provide an optimal combination of the final functional IC, it is also the objective of the subject invention to provide an

infrastructure standard enabling the different functional blocks, each may have a variation of specifications, to be selected by the application engineer in accordance with the product requirements of a project. Technically it is also possible to provide a combination of selected functional blocks to compose a single IC chip through an ASIC Application Specific IC design process if these circuits belong to the same type of IC fabrication technology. Functional blocks of circuits are selected and combined to form a final single chip IC. However, the ASIC chip concept has several drawbacks: The product development time is substantially longer than the development process using an off the shelve micro-controller. Engineering prototype is more expensive and takes longer time to obtain. Production lead-time of the ASIC chip is also substantially longer than commercial programmable chips, because wafer bank cannot be prepared prior to receiving production order. Short development cycle time and production lead-time are particularly important because in the existing business world, product life is becoming shorter and shorter due to rapid changes of market conditions. On the other hand, standard micro-controller ICs are commodity items available in smaller quantities. Whenever there is a design feature change, possibly affecting the circuit of only one functional block inside the ASIC chip, the whole design and production cycle need to be restarted. Whenever a design bug is found in any one of the functional blocks, the whole ASIC chip is to be scrapped. More important, the recover time to deliver another ASIC chip is also intolerably long especially when the bug is discovered at the time the product is about to be shipped. For timing critical applications, real time applications or projects that require a lot of controller resources, it is often found that the resources of the controller inside the ASIC chip is not adequate to handle all the jobs. The controller resource is particularly tight when more functions or functional blocks are added into the ASIC design. Providing at least one universal central controller ICs, each having one or more communication channels; 2. Other further desirable features of the VSFB system includes: Specifying the communication channel to be a standard high speed serial communication port; 2. The power lines of each VSFB IC is connected to the source points of the power supply to firstly minimize power line common mode noise; and secondly, prevent over designing the power supply of the central controller; 3. After compiling the program, different executable codes are generated for the different processors of each VSFB IC; 4. The communication speed for different VSFB ICs may be different to facilitate timing management of the central controller; alternately the less busy VSFB IC may communicate with the central controller with occasional burst of data through the serial communication link; 5. Since the VSFB ICs are closely located to the central controller on the COB and there is no power requirement in the communication interface, the noise immunity requirement between the communication interface is of much less weight as compared with traditional printed circuit board assembly design. Accordingly it is recommended to make use of a RSCI reduce signal communication interface technique to reduce the level of electromagnetic interference EMI and enabling the final product to easier passing the requirements of FCC. For the benefits of the consumer, it is highly desirable to implement the VSFB technology with a business model that defines an industrial recognized standard for the communication interface, so that different VSFB ICs supplied by different vendors can be used on the same COB design. This standard is particularly important for the RSCI interface specification because of the reduced noise margin of the chip design. An industrial standard is defined by having at least two different companies to provide VSFB ICs to work on the same interfacing design specification. It should be noted that the standard is preferred to cover the software programming specification as well; 7. To further reducing the cost of the system, daisy chain connection of the serial interface among RSCI chips is enabled. In this case, one high speed serial port on the central controller may be adequate for most applications. The most busy VSFB IC should be connected closest to the central controller to minimize signal delay and also to further reduce electromagnetic coupling interference. The principle is to reduce the noise immunity capability of the interfacing circuit by reducing the interfacing signal current or the interfacing signal voltage amplitude of the communication channel connecting between two ICs. This is against the traditional wisdom of designing a communication channel connecting two different components or two different equipments that driving capability of communication ports should be as high as affordable. A lower interfacing current or signal voltage will result in less RF power transmitted. For example, the traditional digital signal amplitude between a serial interface connecting between two ICs operating at 5V is usually around 3. The RSCI circuit

intentionally introducing a voltage drop circuit to reduce the communication circuit voltage to 0. The degree of signal voltage to be reduced is limited by the voltage variation of the application circuit, and also the maximum distance between the two dices on the COB. It should be noted that the example illustrates the concept of RSCI in voltage form, the same RSCI principle is applicable on current form as well; that is to provide full voltage swing but much lower current driving capability between the transmission end and the receiving end. This current is unable to provide sufficient noise immunity under normal communication condition such as the communication interface in between computer and the peripherals but be adequate for interfacing COB VSFB designs.

INTEGRATED FUNCTIONAL BLOCKS pdf

2: Integrated circuit chip with "bit-stacked" functional blocks. - IBM

Abstract Principles of integrated-circuit technology are considered along with elements of integrated functional blocks, models of transistors and diodes for integrated functional blocks, principles of integrated-circuit design, and principles of the theory of sensitivities and tolerances.

The bulk device region has a first device-fabrication surface in which a bulk device is positioned on the bulk growth layer. The SOI device region has a second device-fabrication surface in which an SOI device is positioned on the silicon layer. The first and second device-fabrication surfaces are positioned at a substantially uniform level. Description This patent application is based upon and claims the benefit of the earlier filing date of Japanese Patent Application No. Field of the Invention [] This invention relates to a semiconductor chip having a functional block positioned in an SOI silicon-on-insulator region and another functional block positioned in a bulk region in a single chip and a method for fabricating such a semiconductor chip. Description of Related Art [] DRAM chips having a 1T1C 1-transistorcapacitor memory cell structure have been widely used as an inexpensive and large-capacity memory suitable for high-density integrated circuits. In recent years, demand has been increasing for a system LSI, in which a DRAM and a logic core are integrated in a single chip in order to improve system performance. Such SOI devices have already been mass-produced for use in high-performance logic circuits. However, this method increases the occupied area of both the memory cell and the sense amplifier greatly, and spoils the high integration feature, which is the main characteristic of a DRAM. With this method, oxygen is implanted in predetermined positions in the silicon bulk substrate to produce an SOI structure that coexists with the silicon bulk region. In this method the epitaxial layer is grown until it exceeds the mask layer placed over the SOI substrate region, and then it is planarized using the mask layer as a stopper. In addition, volume expansion that occurs when the buried oxide is formed by reaction between silicon and the implanted oxygen in a thermal process causes stress, and crystal defect is produced at the boundary between the SOI substrate region and the bulk region. Such an interface state and crystal defect are due to contamination and shifting of crystal orientation. This level difference makes it difficult to guarantee the focusing margin in the photolithography process, and to control the height of the buried insulator in the trench when forming isolations. This problem is caused by the fact that crystal grows from both the top face of the base substrate and the sidewall of the SOI layer during the formation of the bulk growth layer. The crystal characteristic of the epitaxial layer having grown from the etched side face of the SOI substrate is inherently bad. In addition, the crystal orientations of the epitaxial layers having grown from the top surface of the base substrate and from the sidewalls of the SOI layer are mismatched with each other at the interface between them further deteriorating the crystal characteristic. Such stress may cause change in the mobility of the carriers and crystal defect. If a transistor is positioned in an area having crystal defect, the device characteristic becomes inferior. Furthermore, because the epitaxial growth layer is polished using the mask layer as a stopper, the final level of the epitaxial growth layer close to the boundary in the bulk region becomes higher than the SOI layer of the SOI substrate region equivalent to the thickness of the mask layer. To avoid the surface unevenness, a troublesome after-treatment, for example, re-polishing the epitaxial growth layer after thinning the mask layer, must be carried out. If the epitaxial growth layer is set broad in order to form a DRAM macro in it, dishing, which is a phenomenon where a center portion of the layer sinks, occurs. The unevenness of the top surface remains as a step or a level difference in the subsequent processes, and adversely affects the manufacturing process. The bulk device region has a first device-fabrication surface in which a bulk device is fabricated, and the SOI device region has a second device-fabrication surface in which an SOI device is fabricated. The first and second device-fabrication surfaces are positioned at substantially the same level. The semiconductor chip 10 has a bulk device region 11, in which circuit elements are positioned in the bulk substrate domain, and an SOI device region 12, in which circuit elements are positioned in the SOI substrate domain. The semiconductor chip 10 is a so-called system-on-chip having multiple functional blocks in a single chip. In the SOI device region [] 12, transistors are formed in the silicon layer i. The SOI device region 12 is suitable for fabricating circuit elements that require high-speed operations

with low power consumption because the insulator exists directly below the active layer, thereby reducing the junction capacitance. Examples of such a high-speed circuit element include a logic device. On the other hand, the bulk device region 11 is suitable for fabricating those devices that require a bulk structure in order to avoiding the floating body effect and the associated problems. Examples of such devices include a DRAM cell and a sense amplifier. In order to realize the system-on-chip shown in FIG. In such a case, the margin space, in which devices cannot be formed, is dead space, and consequently, the chip size becomes large. Meanwhile, it is desirable to eliminate the level difference between the epitaxial bulk region and the SOI substrate region, and to form circuit elements at a uniform level in both regions. The semiconductor chip 10 includes a base substrate 21, a bulk device region 11 located on a part of the base substrate 21, an SOI device region 12 located on the other part of the base substrate 21, and a polysilicon layer 47 located at the boundary between the bulk device region 11 and the SOI device region The bulk device region 11 has a bulk growth layer 26 positioned on the base substrate 21, in which devices are fabricated. The SOI device region 12 has a buried oxide 22 positioned on the base substrate 21, and a silicon SOI layer 23 located on the buried oxide 22, in which devices are fabricated. In the example shown in FIG. These devices and circuits as a whole constitute a DRAM macro as a functional block. Accordingly, the devices or the circuit elements located in the bulk device region 11 and those in the SOI device region 12 are positioned at substantially the same level. The boundary layer 47 between the bulk device region 11 and the SOI device region 12 is polysilicon layer in the example shown in FIG. In order to reduce the number of fabrication steps, it is preferable to use a gate material for the devices 43, 44, and 45 as the boundary layer In this case, the boundary layer 47 can be provided via a gate dielectric film. The top face of the polysilicon boundary layer [] 47 slightly retreats from the epitaxial growth layer 26 and the SOI layer 23 in the example of FIG. However, the boundary layer 47 may project from the surface of the epitaxial growth layer 26 and the SOI layer 23 up to the height of the gate 39 a, 39 b, and 41 of the devices 43, 45, and 44, as indicated by the ghost line in FIG. The gate electrodes 39 a, 39 b, and 41 may further have a silicide deposited on the polysilicon. The semiconductor chip [] 10 also has first isolations 35 a isolating the devices 43 and 44 in the bulk device region 11, in which the DRAM macro is formed, and second isolations 35 b isolating the devices 45 in the SOI device region 12, in which the SOI logic is formed. The first isolation 35 a in the bulk device region 11 and the second isolation 35 b in the SOI device region 12 are almost the same depth. To reduce the number of fabrication steps, it is desirable that the first and second isolations 35 a and 35 b are formed at the same time. In the example show in FIG. However, if the buried oxide 22 is not as thick, the second isolation 35 b may reach through to the silicon base substrate 21 as long as it is substantially as deep as the first isolation 35 a, penetrating the SOI layer By setting the second isolation 35 b to be as deep as the first isolation 35 a, the effective distance between two adjacent devices 45 located in the SOI layer 23 with the second isolation 35 b between them is lengthened. This arrangement can realize miniatured isolation with little leakage current from the interface of the damaged buried oxide 22, and prevent deterioration of the endurance of the second isolation 35 b due to the current leakage. If the first and second insulators are of the same depth and made of the same material, they can be fabricated at once with a sufficient margin under the same condition. The sidewall protection film 25 is, for example, silicon nitride Si3N4 or silicon dioxide SiO2. After such a material is deposited over the entire surface, only the sidewall protection film 25 is left by RIE. Then, after a predetermined pretreatment, a single crystal silicon layer 26 is formed on the exposed silicon base substrate 21 by selective epitaxial growth e. If the sidewall protection film [] 25 is made of silicon nitride Si3N4 in the previous step, process controllability is improved. In the first embodiment, the sidewall protection film 25 is to be removed in a later step. Accordingly, even if the sidewall protection film 25 is made of Si3N4, it will not cause serious stress near the boundary in the final product, and priority can be given to process controllability. If the former mask pattern 24 is made of Si3N4, it can be removed using phosphoric acid. If the former mask pattern 24 is made of SiO2, it can be removed by hydrogen fluoride HF. The sidewall protection film 25 can also be etched depending on the material; however, the etched portion is to be filled with the new mask layer 27, which is also made of SiO2, Si3N4, or a composite layer of these materials. The mask layer 27 is patterned, and the DRAM trench capacitor 30 is formed using the mask pattern 27 using a technique desired. For example, a trench is formed by RIE or other suitable

methods, a lower diffusion plate electrode 31 is formed, and the trench is filled with, for example, n-type polysilicon via a dielectric film not shown to form a storage electrode A collar oxide 32 is formed, and the trench is further filled with polysilicon. To be more precise, the mask layer 27 is patterned, and trenches with the same depth are formed for isolation in both the bulk device region 11 and the SOI device region These trenches are filled with an insulator using the masks 27 as stoppers. In this manner, the first isolations 35 a in the bulk device region 11 and the second isolations 35 b in the SOI device region 12 are formed at the same time. If an etching condition that silicon and silicon dioxide are etched at the same etching rate is set, the trenches for the first and second isolations in the bulk device region [] 11 and the SOI device region 12 can be dug at the same rate until the trenches reach the depth necessary to make the isolations between the straps 33 of the DRAM cells, between transistors of the peripheral circuit, and between the SOI devices. The trenches are then filled with the same dielectric material, thereby completing the first and second isolations 35 a and 35 b. The mask layer 27 is also removed. Even in case that the sidewall protection film 25 remains, it is removed during the removal of the mask layer 27 and in an additional etching process carried out if necessary, and a recess 46 is formed. Then, the recess 46 is filled with a silicon group material to produce the boundary layer 47 shown in FIG. Filling the recess 46 may be carried out as an independent step, or alternatively, the recess 46 may be filled up when gate electrodes 39, 41 are formed. In the former case, wells and channels are formed, if necessary, using an ion implantation technique after the recess 46 is filled. Gate electrodes 39, 41 are formed via the gate dielectrics 48, and source and drains 40 and 42 are formed. In the latter case, the gate electrodes 39, 41 are made of a silicon group material, such as polysilicon or SiGe, and the recess 46 is automatically filled with the gate material when forming the gate electrodes. In either case, the SOI layer 23 is coupled with the single crystal silicon epitaxial growth layer 26 via the same silicon group material between them. After the gate electrodes [] 39, 41 are fabricated, interlevel dielectrics and interconnections are formed according to a desired MOSFET fabrication process. If a salicide is provided over the gate electrodes and sources and drains when forming transistors, it is preferable to protect the boundary with a mask in the structure shown in FIG. If the polysilicon layer 47 projects from the device-fabrication surface overlapping the source and drain, the recess is protected by the polysilicon itself, and therefore, salicide process can be carried out without an additional protection mask. Accordingly, the pn junction of the strap 33 and the source and drain of the DRAM cell 43 can be positioned shallower than the interface between the base substrate 21 and the epitaxial growth layer 26 for the purpose of reliably separating the pn junctions from the interface. This arrangement can prevent junction leakage and maintain the retention characteristic of the memory cell, even if the interface state deteriorates due to process conditions. Since, in the first embodiment, the epitaxial growth layer [] 26 of the bulk device region 11 ad the SOI layer 23 of the SOI device region 12 are coupled with each other via a silicon group material, such as polysilicon or SiGe, stress at the boundary is reduced. Consequently, crystal defect due to stress is prevented. Changes in mobility due to stress between two regions are also prevented, and those devices located near the boundary can be effectively protected from deterioration. In addition, the device-fabrication surfaces of the bulk device region and the SOI device region are located at the same level, which is advantageous for the subsequent processes for fabricating trench isolations and gate electrodes using a lithography technique. Consequently, the second isolation in the SOI device region 12 can effectively prevent leakage current from the interface of the buried oxide. The system-on-chip shown in FIG. Using the fabrication method of the first embodiment, the isolations in both the bulk device region and the SOI device region, whose device-fabrication surfaces are at substantially the same level, are formed at once at the same etching rate so as to have the same depth. Accordingly, the process conditions, such as the thickness of the dielectric for filling the trench and the etchback time, are substantially the same over the bulk device region and the SOI device region. Consequently, the process for fabricating the isolations is simplified. The semiconductor chip 50 includes a base substrate 51, a bulk device region 11 having an epitaxial growth layer 56, and an SOI device region 12 having, a buried oxide 52 positioned on the base substrate 51 and an SOI layer 53 on the buried oxide The bulk device region 11 has a first device-fabrication surfaces, in which devices 43, 44 are positioned. The semiconductor chip 50 also includes a first isolation 65 a isolating the devices 43, 44 in the bulk device region 11, a second isolation 65 b isolating

the SOIMOSFETs 45 in the SOI device region 12, and a third isolation 65 c located at the boundary between the bulk device region 11 and the SOI device region In this embodiment, the third isolation 65 c is the boundary layer. The first, second and third isolations [] 65 a, 65 b, and 65 c are of the same depth and made of the same dielectric material.

3: Formats and Editions of Integrated functional blocks [www.enganchecubano.com]

Integrated functional blocks: 6. Integrated functional blocks. by Mirko NovÃ¡k Print book: English. Amsterdam ; New York: Elsevier Scientific Pub. Co ; Prague.

Expandable communication system with data flow control Star coupler device including means for connecting multiple star couplers together in a cascaded relationship Attorney, Agent or Firm: A circuit arrangement 10 for interfacing a plurality of functional blocks 22, 24, 26, 28 to one another within an integrated circuit device, said functional blocks contained within the integrated circuit device, the circuit arrangement 10 comprising: The circuit arrangement 10 of claim 1, further comprising a plurality of port interfaces 30, 32, 34, 36, 38 , each port interface disposed within and coupled to a functional block to interface the functional block with the serial port associated therewith. The circuit arrangement 10 of claim 1, wherein the serial command and data interconnects for at least one of the serial ports respectively include serial command and data input lines. The circuit arrangement 10 of claim 1, wherein the serial command and data interconnects for at least one of the serial ports respectively include serial command and data output lines. The circuit arrangement 10 of claim 1, wherein, for at least one of the serial ports, the serial command interconnect thereof includes separate serial command input and output lines, and the serial data interconnect thereof includes separate serial data input and output lines. The circuit arrangement 10 of claim 1, wherein, for at least one of the serial ports, the serial clock interconnect thereof includes separate serial clock input and output lines. The circuit arrangement 10 of claim 1, wherein the serial command and data interconnects for at least one of the serial ports are differential interconnects. The circuit arrangement 10 of claim 1, wherein the serial command and data interconnects for at least one of the serial ports are single-ended interconnects. The circuit arrangement 10 of claim 1, wherein the interface controller 14 is configured to selectively couple serial ports to one another responsive to a controller command received from a functional block via the command interconnect of the serial port associated therewith. The circuit arrangement 10 of claim 9, wherein the interface controller 14 is further configured to direct functional block commands between source and target functional blocks via the command interconnects of the serial ports associated therewith to permit the source functional block to control the target functional block. The circuit arrangement 10 of claim 9, wherein the interface controller 14 is further configured to establish the logical communications channel by receiving a channel request received from a requesting serial port, forwarding a channel request to at least one target serial port, receiving a connect response from the target serial port, and forwarding a connect response to the requesting serial port. The circuit arrangement 10 of claim 11, wherein the interface controller 14 is further configured to establish a logical communications channel requested by the requesting serial port only in response to a grant indication in the connect response from the target serial node, and to refuse establishment of a logical communications channel requested by the requesting serial port responsive to a deny indication in the connect response from the target serial node. The circuit arrangement 10 of claim 11, wherein the interface controller 14 is further configured to release at least one serial port from a logical communications channel in response to a channel abort command received from one of the plurality of serial ports. The circuit arrangement 10 of claim 9, wherein the interface controller 14 is configured to selectively preempt a logical communications channel responsive to a channel request received from a requesting serial port having a higher priority than at least one of the serial ports coupled to the logical communications channel. The circuit arrangement 10 of claim 1, wherein the interface controller 14 is further configured to direct an interrupt command between a source and a target functional block to permit the source functional block to preempt a logical communications channel established for the target functional block. The circuit arrangement 10 of claim 1, wherein the interface controller 14 is configured to selectively couple a source serial port to at least two target serial ports to define a broadcast logical communications channel between the functional blocks associated therewith. The circuit arrangement 10 of claim 1, wherein the interface controller 14 is configured to selectively couple at least another two of the plurality of serial ports to one another to define a second logical communications channel between the functional blocks associated therewith, the interface controller further configured to concurrently transmit information over the first and

second logical communications channels. The circuit arrangement 10 of claim 17, wherein at least one of the serial ports includes serial command and data in lines and serial command and data out lines, and wherein the interface controller 14 is configured to couple the serial command and data in lines to the first logical communications channel, and to couple the serial command and data out lines to the second logical communications channel. The circuit arrangement 10 of claim 1, wherein the interface controller 14 includes a programmable arbitration scheme. The circuit arrangement 10 of claim 19, wherein the interface controller 14 is configured to receive arbitration data 67 defining the arbitration scheme from at least one of the plurality of serial ports. An integrated circuit device comprising the circuit arrangement 10 of claim 1. A data processing system comprising the circuit arrangement 10 of claim 1. A program product, comprising a hardware definition program that defines the circuit arrangement 10 of claim 1 and a signal bearing media bearing the hardware definition program. The program product of claim 23, wherein the signal bearing media includes at least one of a transmission type media and a recordable media. A method of interfacing a plurality of functional blocks 22, 24, 26, 28 in an integrated circuit device, said functional blocks contained within the integrated circuit device, each functional block associated with and coupled via one point-to-point serial interconnect 50, 52, 54, 56, 58 to one of a plurality of serial ports 40, 42, 44, 46, 48 under the control of an interface controller 14 , each serial port including separate commands, data and clock interconnects, the method comprising: The method of claim 25, wherein each serial interconnect 50, 52, 54, 56, 58 includes separate serial command and data lines. The method of claim 25, wherein communicating data between the first and second functional blocks includes directing functional block commands between the first and second functional blocks over the logical communications channel. The method of claim 25, establishing the logical communications channel includes: The method of claim 28, wherein establishing the logical communications channel further includes determining whether the connect response from the second functional block includes a grant indication. The method of claim 29, further comprising: The method of claim 28, further comprising releasing at least one of the first and second functional blocks from the logical communications channel in response to a channel abort command received from one of the plurality of functional blocks 22, 24, 26, The method of claim 28, further comprising selectively preempting the logical communications channel responsive to a channel request command received from a third functional block having a higher priority than at least one of the first and second functional blocks. The method of claim 25, further comprising: The method of claim 33, wherein selectively preempting the logical communications channel includes: The method of claim 25, wherein establishing the logical communications channel further includes coupling a third functional block to the logical communications channel. The method of claim 25, further comprising programming the interface controller 14 with an arbitration scheme. The method of claim 37, wherein programming the interface controller 14 includes receiving arbitration data 67 defining the arbitration scheme from at least one of the plurality of functional blocks 22, 24, 26, Field of the Invention The invention is generally related to integrated circuit device design and architecture, and in particular, to an interface for interconnecting multiple functional blocks together in an integrated circuit device. Background of the Invention Computer technology has advanced a great deal over the last several decades. The size and number of logic gates that can be integrated together on a chip continues to improve, and whereas early chips had at most only a few hundred gates, more recent chips have been developed that incorporate more on the order of millions of gates. Furthermore, advances in integration have permitted designs that were at one time implemented using multiple chips to be implemented in a single chip. As chip designs become more complex, however, the design and development process becomes more expensive and time consuming. To alleviate this difficulty, design tools have been developed that enable developers to build custom chips by assembling together smaller, generic components that perform basic functions required for the design. By using generic components, design time and effort are reduced, since circuits do not need to be designed gate by gate. Moreover, the components usually can be tested and optimized prior to assembly in a particular design, so that the testing effort placed on the developer of an overall design is substantially reduced. The ability to integrate greater numbers of gates onto a chip has also permitted the complexity of the generic components used by design tools to increase. Whereas early generic components replicated basic functions such as multiplexers, registers, counters, etc. These more

advanced components are referred to herein as functional blocks, insofar as they are configured to perform one or more high level functions in a design. Functional blocks typically are portable to the extent that they are reusable in different designs. Moreover, they are often autonomous, and thus capable of operating independently and concurrently with other components in a design. One difficulty associated with the use of components such as functional blocks arises from the need for the various components in a design to communicate with and transfer information among one another. Each component typically has one or more interfaces defined therefor through which communication with other components, or with other devices external to a chip, is handled. These interfaces are typically interconnected with one another over an interconnect system such as a bus to support communication between the different components. For example, one common manner of interconnecting multiple components is through the use of a multi-drop bus. With a multi-drop bus, each component is coupled to a common set of lines, so that each component is capable of receiving every communication passed over the bus. Information passed over a bus is usually associated with a particular address or other identifier so that, only the component that is the target of the information actually receives and processes that information. The other components that are not targeted for the information ignore the information. Typically, a bus is parallel, incorporating multiple lines so that multiple bits of information can be transmitted simultaneously. Moreover, both control information, used by one component to control the operation of another component, and data, representing the information being manipulated by the components, are typically sent over the same lines in the bus. For example, one bus architecture used in integrating multiple functional blocks in a chip is the Peripheral Component Interconnect PCI bus architecture, which is more conventionally used at the board level to interconnect a microprocessor with different peripheral devices in a computer. However, bus-type interconnections suffer from a number of drawbacks that limit their usefulness in interconnecting multiple functional blocks in a chip. First, parallel bus architectures require a relatively large number of lines, or wires, to run between the various components connected to the bus. Routing wires between components can take up valuable space in a design and reduce the number of components that can fit into the design. Many parallel buses, for example, transmit data in or bit words, requiring at a minimum 32 or 64 lines to be routed to each component, not counting any additional control signals that may be required. Second, typically only one component can transmit information over a parallel bus at a time. Therefore, other components that desire to transmit information typically must wait until that component is done transmitting its information, or in the alternative, each component must share the bus and transmit pieces of information one after another, which slows down the transmission rate for all components. Also, control information and data typically share the same lines in a parallel bus, and as a result, control operations that might otherwise be capable of being performed within a particular component without requiring access to the bus may have to wait until a data transmission, started prior to the desired control operation, is complete. Third, the overall speed of a parallel bus may be limited, and thus limit the potential bandwidth of information that can be communicated between components. Bandwidth in a parallel bus is typically improved by increasing the width of the bus or increasing the clock speed of the bus. Increasing the width, however, adds additional lines to the bus, thus adding to the routing density of the design. Increasing the clock speed, on the other hand, may limit the number of components that can be attached to the bus, since the number of components can affect the amount of load and routing parasitics on the bus, each of which limits permissible clock speed. US Patent 5,, discloses an integrated circuit device including first and second level star couplers. The first level star coupler includes a plurality of inputs and corresponding outputs and functions to logically OR together all signals received at its inputs to generate a first output signal. The second level star coupler also includes a plurality of inputs and corresponding outputs, one of the inputs to the second level star coupler being connected to receive the first output signal. The second level star coupler functions to logically OR together all signals received at its inputs, including the first output signal, to generate a second output signal which is provided at each of its outputs. A switch or multiplexer directs either the first or second output signal to each one of the outputs of the first level star coupler. Within such a system, interconnections of input signals to outputs is restricted in accordance with the conventions of star coupling. Therefore, a significant need exists in the art for an improved manner of interconnecting components such as functional blocks and the like in an integrated circuit

design, and in particular, for a manner of interconnecting components that is more flexible, compact, fast, reusable, and expandible than conventional designs. Summary of the Invention The invention addresses these and other problems associated with the prior art by providing a circuit arrangement and method that interface multiple functional blocks within an integrated circuit device via a concurrent serial interconnect that is capable of routing separate serial command, data and clock signals between functional blocks in the device. According to a first aspect of the invention, there is provided a circuit arrangement for interfacing a plurality of functional blocks to one another in an integrated circuit device, said functional blocks contained within the integrated circuit device, the circuit arrangement comprising: According to a second aspect of the invention, there is provided a method of interfacing a plurality of functional blocks in an integrated circuit device, as defined in independent claim A concurrent serial interconnect consistent with the invention utilizes a plurality of serial ports that are selectively coupled to one another by an interface controller to define one or more logical communication channels between two or more of the serial ports. The logical communication channels in essence function as point-to-point serial interconnections between functional blocks, so that direct communications between logically connected functional blocks can occur. Through the use of serial interconnects, the number of lines required to be routed to and from individual functional blocks is reduced, thereby simplifying the integration of functional blocks into a design and reducing the routing congestion associated with inter-block communication. In addition, by communicating via separate serial command, data and clock signals, high speed data throughput can be supported. Furthermore, should more than one logical communication channel be supported by an interface controller consistent with the invention, multiple communication sessions can occur in parallel, thereby further increasing overall data throughput. Another benefit of a concurrent serial interconnect consistent with the invention is that the design of integrated circuit devices and the like is substantially simplified. Functional blocks may be assembled together through the addition of a serial interconnect, with each functional block associated with one of a plurality of serial ports in the serial interconnect by routing separate serial command, data and clock wires therebetween. Design and development is simplified as the addition of new functional blocks to a design typically affects only the design of the serial interconnect, and specifically, the interface controller used therein. Moreover, modular testing and verification is facilitated insofar as communications between functional blocks primarily passes through the serial interconnect, and the need for testing and verifying individual interconnections between functional blocks is often reduced or eliminated. Further embodiments of the invention are specified in the appended dependent claims. These and other advantages and features, which characterize the invention, are set forth in the claims annexed hereto and forming a further part hereof However, for a better understanding of the invention, and of the advantages and objectives attained through its use, reference should be made to the Drawings, and to the accompanying descriptive matter, in which there is described exemplary embodiments of the invention. FIGURE 4 is a flowchart illustrating the sequence of operations performed during a system reset by the interface controller of Fig. FIGURE 5 is a flowchart illustrating a sequence of operations performed when establishing a logical communication channel in the circuit arrangement of Fig. FIGURE 6 is a flowchart illustrating a sequence of operations performed when releasing a logical communication channel in the circuit arrangement of Fig. FIGURE 7A, 7B and 7C are timing diagrams respectively illustrating exemplary data stream transmissions between two ports during establishment of a logical channel, processing of a read request over the established channel, and release of the channel. FIGURE 8 is a flowchart illustrating a sequence of operations performed during an implicit preemption operation for the circuit arrangement of Fig. FIGURE 9 is a flowchart illustrating a sequence of operations performed during an explicit preemption operation for the circuit arrangement of Fig.

4: Block Center for Integrative Cancer Treatment, Chicago

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In this way â€" and with its impact on all aspects of life, work and emotional well-being â€" cancer affects people on all fronts. A recognized leader and pioneer in integrative cancer treatment, the Block Center sets the standard for true integration of multiple science-based strategies that, together, can help you beat the odds and put life over cancer. Learn More Leaders in promoting life over cancer. Led by Keith Block, MD and Penny Block, PhD, our team of cancer professionals provides a different kind of cancer care that emphasizes life, individualized treatment and a multifaceted approach. Keith Block is known around the globe for his pioneering work and leadership in integrative cancer treatment, and Penny Block, PhD is an expert in the biobehavioral aspects and comprehensive lifestyle approaches essential to cancer care. Meet Our Team Making the most of conventional cancer therapies. Chemotherapy, radiation treatment and surgery are not the only forms of cancer treatment. But research affirms that they can be highly effective, important therapies which help improve and save lives. At the Block Center for Integrative Cancer Treatment, our approach is to integrate into your care those treatment strategies that science shows help against cancer. So surgery, radiation and chemotherapy are among the options we will consider and discuss with you as ways within our comprehensive system of care to help you beat cancer. Comprehensive, Detailed Testing For More Informed, Effective Cancer Treatment Although you have a particular type and stage of cancer, it affects you as an individual in distinctive ways that depend on your unique biology and clinical condition. We perform a comprehensive, integrative assessment of your personal biochemistry and the metabolic and molecular characteristics of your cancer. The human body has rhythms and cycles â€" sleep, feeding, hormone production, cell regeneration and other cycles â€" revolving around the hour day. Science shows that these cycles are unique for everyoneâ€¦ and that they influence the effectiveness and toxicity of anticancer treatments. So we pioneered equipment and protocols that optimize the timing and rate of treatment delivery thereby reducing toxicity and side effects and maximizing treatment efficacy. How you eat â€" what you put into your body â€" affects your metabolism, health, physical function and, yes, your cancer. And there are certain foods and nutritional supplements that can help make your body less hospitable to cancer. Others â€" sugar, for example â€" help fuel the cancer. So, rather than an afterthought, nutrition is an integral, and entirely individualized, part of our approach to treating cancer. In fact, science has long demonstrated that mental, emotional and behavioral factors affect biology, and influences the success of treatment. Our all-fronts approach to fighting cancer includes a robust biobehavioral care program led by Penny Block, PhD. We work to understand and address your personal challenges and emotional needs in order to help you stand up strong against cancer with the best odds for treatment success. At the Block Center, we offer a unique program designed to prevent cancer recurrence. They provided the best of conventional cancer treatment integrated with a whole host of science-supported therapies and services that helped me win my fight. They gave me a lot of hope. After just 6 months, my tumor markers have dropped from over to just 2. I wanted to do everything possible to keep that fate off the table. I wanted a long, satisfying life, and I felt the Block Center would give me the best opportunity for that. Four years since my diagnosis of Stage 3B colon cancer, there are no signs of cancer in my tests and nothing indicating cause for concern.

INTEGRATED FUNCTIONAL BLOCKS pdf

5: Function block diagram - Wikipedia

based on integrated functional blocks Alberto Castellazzi, Adane Kassa Solomon, Nicola Delmonte, Member, IEEE, and Paolo Cova - packaging bases on the identification of functional blocks.

An integrated circuit chip 10 for large scale integration of a data processing application comprising a number of functional blocks L1 2 to L36, C60 to C80 and R90 to R with an n-bit wide data flow path for transferring a data word having n-bit positions from an n-stage source functional block to an n-stage destination functional block on said chip through at least one other n-stage functional block in said data flow path; said chip being characterized in that: The chip according to Claim 1 in which said functional blocks have a relatively high percentage of the total semiconductor devices embodied on said chip The chip according to Claim 1 or 2, in which said blocks are arranged in stacked arrays which are disposed parallel to each other on said chip The chip according to Claim 1, 2 or 3 in which said functional blocks include at least one said block which functions as as data storage register L15, L16 and at least one said block that functions as a multiplexor L22, L25 or L The chip according to claim 4 in which said data storage register block L15 has a latch circuit in each said stage. The chip according to Claim 5 in which said latch circuit comprises a plurality of semiconductor devices which are interconnected to form a polarity hold function. The chip according to Claim 6 in which each said latch circuit is interconnected to an adjacent latch circuit to permit said circuits to be LSSD tested. The chip according to Claim 7 in which said latch circuit includes an input terminal and said stage further includes an input multiplexor for selectively switching one of a plurality of input signals to said input terminal in response to different control signals supplied to said input muihplexor. The chip according to claim 6, 7 or 8 in which said plurality of semiconductor devices are FET type transistors. The chip according to Claim 9 in which some of said FET type transistor in selected stages of predetermined blocks are interconnected by said conductors 40 disposed on said at least one conductive layer. The chip according to any one of claims 3 or 5 to 10 in which at least one of said stacked arrays extends from one side of said chip to the opposite side of said chip and includes at least 20 functional blocks. The chip according to any one of the preceding claims in which said plurality of conductors 40 in said at least one conductive layer are allocated to establish the plurality of "n" conductor buses and in which said plurality of buses are arranged in at least one group having at least 7 buses which may be employed for global wiring. The prior art has disclosed various arrangements for implementing on an integrated circuit chip, circuits that process binary data. While the arrangements all have the same general objective of providing low cost function on each chip, the manner in which the devices are interconnected to form circuits and these circuits are then interconnected to form higher level functional blocks varies as different pnbnties are placed on the various factors that influence this cost. For example, the layout, meaning the position of the semiconductor devices and their interconnections, for two chips each implementing the same complex logical control function and each employing the same basic semiconductor technology can differ substantially if the first places a high degree of emphasis on reducing development cost and the second places a high degree of emphasis on reducing volume manufacturing cost. One of the main reasons for this difference is the set of constraints imposed by such emphasis on the method of providing for the global wiring pattem which interconnects circuits and blocks. In some integrated circuit arrangements of complex logical control functions, automatic procedures are employed to produce the layout of the circuits and the wiring. Since both the layout and the wiring must follow prescribed rules in this approach, compromises are made between the wirability of the chip and the number of circuit devices per chip and, quite often, less than optimum integration is achieved. In other integrated circuit arrangements, the chips start out with a basic organization of devices and are later personalized by wiring in the last stages of the process to implement a specific logical function or system. While this makes the overall process economical from a development cost per chip standpoint, it frequently results in the need to employ a number of chips to implement a function that, with proper planning from the beginning, could have been implemented on a single chip. Hence, the apparent economic saving is lost and overall system performance is degraded by the additional buffering needed to boost signal levels through these unwanted chip to chip connections. It is therefore highly desirable in

performance andlor manufacturing cost oriented designs to provide as much function on one chip as possible. A chip layout of circuits done on a custom basis can, in theory, result in the most densely packed layout of circuits and wiring. However, this is no longer practical at the present level of large-scale integration because of the extremely large number of circuits involved unless the chip is partitioned into functional blocks. Moreover, for this latter approach to be schedule and development cost competitive, it is very desirable that many of these functional blocks belong to a family of predesigned units which can be used on more than one chip. It is therefore an object of the present invention to provide an integrated circuit chip that is highly integrated and avoids costly and performance degrading chip to chip connections. A second object of the present invention is to provide an improved layout for an integrated circuit chip which is implementing a system that comprises a relatively high proportion of interconnected multistage blocks having different functions. Another object of the present invention is to embody a data handling system, having at least one multi-bit data flow path involving a plurality of functional blocks on a semiconductor chip in an arrangement which permits a high utilization of the chip area. A further object of the present invention is to accomplish the physical design in a schedule and resource efficient manner by using members of a family of predesigned functional blocks during the design process. It has been found in accordance with the present invention that when the application to be embodied on the chip involves a high proportion of multi-stage functional blocks, such as is normally encountered in certain portions of a data processing system where multi-bit data words are transferred between different parts of the system, an approach referred to as "bit stacking" produces a highly efficient layout of circuits and metalization. In accordance with the "bit stacking" concept, the multi-stage functional blocks all have the same number of stages, with each stage handling or processing one bit of a multi-bit word. Generally in the application under consider- ation, one or more multi-bit data paths exist in the design for transfening a multi bit word, for example 32 bits, between a source functional block through a number of other blocks, perhaps having other functions, to a destination functional block. The present invention teaches that, in this type application, each stage of the functional blocks be designed to have the same physical width even though corresponding stages of blocks having different functions might employ a different number of basic semiconductor devices. If the blocks are stacked vertically on the chip such that corresponding logical stages are aligned and if the order of the blocks reflects, whenever possible, the sequence of the data flow, the implementation of the global wiring in two levels of metalization, as well as the implemention of whatever metal wiring is required for interconnecting devices within a stage and that required in interconnecting these stages within a functional block, is tremendously simplified. This permits a closer packing density of the functional blocks and hence, an integrated circuit package with a relatively high degree of function. Objects and advantages other than those mentioned above will become apparent in the following description when read in connection with the drawing. An important characteristic of the present invention is seen from the plan view of chip 10 in Fig. Chip 10 has a general organization which comprises three columns or stacks, the left stack LS , the center CS , and the right stack RS , each of which compnse a group of functional blocks. The left stack LS comprises the following functional blocks which are listed from the top horizontal side 11 of chip 10 in the order in which they appear in the stack. Each stage of each block also has the same width, "w", and corresponding stages of the blocks in each stack are aligned physically on the chip. The number of stages in each block corresponds to the overall compos he word width of the data flow paths that have been established on the chip to implement a predetermined function of a data processing system. In this instance, the function implemented on the chip is referred to as "address translation" which involves converting a "virtual" memory address to a "real" memory address. The logical arrangement of the blocks shown in Fig. At this point, it is important to understand that the system function that is implemented on the chip 10 is only significant to the invention in that it demonstrates a number of different data flow paths involving a number of functional blocks which perform different processing functions. For example, the left stack LS contains register blocks, multiplexor blocks, check bit generators, parity generators and parity check generators, etc. While the blocks vary in function, they all have the same physical width, "W", determined by the physical width, "w", of the stages and the overall composite word width, "n", of the data flow path. Various blocks in the left stack are interconnected by buses 40 which, as shown, are vertical lines starting at an

output terminal on one block, represented by a small circle or 0 designated by reference character 41 and ending at one or more input terminals of other blocks represented by an X and designated Each bus 40 represents "n" conductors where n is the number of data bits in the data flow path. These buses in practice are formed in the metal one layer of the chip shown in Fig. The center stack CS and right stack RS are arranged in a manner similar to the left stack. The various functional blocks in the CS and RS stack are appropriately labeled with the legends indicating their general function, together with appropriate reference characters which are also employed in the more conventional data flow diagram of Fig. The blocks in the center stack CS and right stack RS are appropriately interconnected by buses 40 as described in connection with the left stack. A second set of buses 50 shown in Fig I is disposed 90 degrees to the vertical buses 40 and functions to interconnect selected blocks in the different stacks by interconnecting different pairs of vertical buses 40 associated with the same stack. The latter interconnection is represented by a square block 43 where the two buses cross. Connections 41, 42, and 43 represent conventional interlayer connections between either the two layers of metalization M1 and M2 in the chip or one layer of metalization and a terminal contact formed on the layer of the actual semiconductor device. The chip 10 is aiso provided with extemal connecting pads around its periphery for providing extemai input and output connections to the chip. It can be seen that a relatively large proportion of chip area is allocated to multistage functional blocks. The overall function of the address translation system as shown in Fig. The chip is basically a storage controller that interconnects the processor storage channel on one side to the main storage on the other side and implements the following three general functions: This logic implements the proper communication protocol from the PSC to the address translation logic and storage controller logic on the chip All communication to and from the PSC is handled by this logic. This logic although fully represented in Fig. I is not supported by an accompanying conventional system block diagram as are the other two generai functions. The second major function is the address translation function shown in Fig. This logic implements the translation from a 32 bit virtual or "effective" address received from the PSC to a real or physical address used to access storage. The low order 12 bits bits of the incoming effective address are used as the byte address within a "real page" the 12 bit address of which is to be determined by the address translation mechanism , and are not altered by the translation process, but are instead directly output to storage from the storage address register C The high order 4 bits bits of the incoming effective address are used to index into a "segment table" 16 x 18 RAM R96 to select 1 of 16 18 bit registers, the contents of which are intermittently updated by an operating system control program. Twelve of the 18 bits of the referenced segment register contain a segment identifier which is concatenated with 12 bits bits of the incoming effective address to form a 24 bit "virtual" address. Bits 16 - 19 of the incoming effective address are used to address two table look-aside buffers TLBs in parallel. The contents of the TLBs are intermittently updated by the controller from a "page table" area maintained in main storage by an operating system program. The address tag field 24 bits of each table look-aside buffer is compared to the 24 bit virtual address which has been formed as described above. If either of the two compares are equal, then the real page number field of the associated table lookaside buffer contains the remaining 12 bits of the real address the real page and is subsequently output to storage as the real page address. These 12 bits, in conjunction with the 12 bits output previously, form the entire real address used to access main storage. The third and last function of the storage control is to provide the address, data, and storage control signals from the controller to the extemal storage. Error detectionicorrection ECC logic, as well as dynamic memory refresh control is also provided by this function. This function is shown in Fig. The main input on the chip 10 for receiving an address from the microprocessor which is to be translated, is at terminal T15 of the input register C Register C68 appears at the top of Fig. Register C68 is a 32 data bit register four additionai bits are used for parity. The four high order bits of the 32 data bits stored in register C68 are applied to the addressing circuit of the segment RAM R96 by bus , a 4 bit output of multiplexor L The 12 bit output bus of the RAM R96 is concatenated with the middle bits of the original address stored in register C68, to form bus The 32 bit output of register C68 on bus is divided and 12 bits of the concatenated virtual address are supplied through the multiplexor L28 on bus The result, com prising 24 bits, is supplied to the comparators L29 and L30 on bus , which is the search argument for the address tag RAMs L33 and L34, each of which supplies a 24 bit comparison word on buses and to the

other input of the comparators L29 and L30 respectively. If a match is found, the translated address high order bits are obtained from the associated real page number RAM R97 or RAM R98 through multiplexor R and are output through bus to a combination off chip drivenimultiplexor located chip periphery CP1. The low order 12 bits of the "real" address are routed to this same peripheral multiplexor through bus from the storage register C77 and have not been translated since they were directly supplied on bus to storage register C77 from terminal T It should be understood that the above description of the translation function is merely to provide a background for an understanding of the relationship of the blocks shown in Fig. The buses involved in the above description have been identified in Figs. The various data flow paths that are established in the chip 10 and the logical organization of the various functional blocks is more readily understood from Figs. It should be understood that the term "data flow path" describes the path that an n bit data word traces when the word is transferred parallel by bit between a pair of blocks, each of which is capable of storing the word, at least temporarily. A segment of the data path, on the other hand, involves a portion of the data flow path involving at least one block at the start or end of the segment where the data word is not stored, such as in a multiplexor. The overail function of the arrangement shown in Fig. In order to better relate a data flow path in Figs. The data flow paths and segments involved in that operation will be traced on both Fig. A PIO function occurs when something has gone wrong in the general system in the address translation function. The data flow path discussed above from the SER register C80 to the PIO multiplexor is indicated by bus , that from R to L31 by bus , that from L31 to L25 by bus , that from L25 to register L1 5 by bus , that from L15 to L14 by bus , that from L14 to register L16 by bus and finally that from register L16 to terminal T13 by bus It must be understood that the PIO function is not performance critical. Assuming that the contents of the output word are anaiyzed by the microprocessor and that this analysis indicates that a page fault has occurred, that is, the data is not in memory but is still on the disk, the processor then issues another PIO command. The system then takes corrective action by loading the proper page from disk memory into main storage and retums the processor to the originai program. The data flow path from the SEAR register C74 through multiplexor C70 to multiplexor C71 to register L16 and finally to terminal Tri 3 is a typical multisegment data flow path which the present invention implements in a very efficient manner.

INTEGRATED FUNCTIONAL BLOCKS pdf

6: Allulose â€“ New Sweetener on the Block - Kara Fitzgerald ND Naturopathic Doctor

The integrated chip (10) includes at least one multi-bit data flow path for transferring data from a source functional block to one or more destination blocks, each functional block performing differe.

Wait N clock cycles. Wait an additional cycle for the instance enable to become stable. In this embodiment, the control circuit comprises a single-bit counter 41 and a pair of AND gates 42 and The input and output signals from the control circuit have the same functions as in the control circuit of FIG. As mentioned above, the transparent paths between functional block ports and chip pads during the test mode are provided by multiplexers. The multiplexer circuits will now be described. As will become apparent in the following, certain of the multiplexers can have as many as N input ports. More particularly, the output of multiplexer 51 is connected to chip pad P. For purposes of discussion, the line carrying the output test signal from block B. In operation of the circuit of FIG. Thus, ordinarily, signals pass unimpeded from circuitry C. However, when the signal on line N[1] goes low i. It should be noted that the delay introduced into the system signal path is only the time taken by the signal to propagate through multiplexer In the illustrated example, the two functional blocks are connected to a two-input multiplexer 53 via respective test test signal lines Test Signal [2] and Test Signal [63]. The multiplexer 53 has a single select line connected to Cnt[0] which assumes different states depending on whether the instance counters contain a count of 2 or a count of Further in the circuit, the output of the multiplexer 53 is connected to an input of a multiplexer 51, as is a system signal ordinarily connected to a particular system connection. The select input of the multiplexer 51 is determined, via AND gate 52, by instance select lines N[2] and N[63]. When one of the signals on select lines N[2] or N[63] goes low, the signal from the multiplexer 53 is directed to the original system connection in place of the system signal. Then, depending upon the state of the count line Cnt[0], the output of the multiplexer 53 will correspond to the signal on one of the test signal lines Test Signal [2] or Test Signal [63]. In the illustrated example, the functional blocks are connected to a multi-input multiplexer-like circuit 53 via respective test signal lines TS[j], TS[k], and TS[l]. Multiplexer circuit 53 receives instance select lines N[j], N[k] and N[l]. Further in the circuit, the output of multiplexer circuit 53 is connected to the second input of multiplexer It should be noted that multiplexer 51 is connected as previously shown except that its select input is determined, via AND gate 52, by instance select lines N[j], N[k], and N[l]. It should also be observed that the delay on the system path equals only the delay through multiplexer 51 and is independent of the number of test signal lines being multiplexed. When one of the signals on select lines N[j], N[k], or N[l] goes low, the signal from multiplexer circuit 53 is directed to the original system connection in place of the System signals. Then, depending upon the state of the instance select lines N[j], N[k] and N[l], the output of multiplexer circuit 53 will correspond to the signal on one of the test signal lines TS[j], TS[k], or TS[l]. In practice, five basic types of connections can be used for providing a transparent path between the port of a functional block and a pad of a host chip: Circuitry to provide each of those connections will now be described. N and an input pad P. In the circuit shown, a 2-to-1 multiplexer 56 is interposed between the unidirectional pad and the port. One input of multiplexer 56 is connected to pad P. The select input of multiplexer 56 is connected to line N62484 where "N" is the number which has been assigned to identify the functional block B. However, when functional block B. N is to be isolated for testing, the binary state of line N62484 changes and, therefore, multiplexer 56 directs signals i. It may be observed that the signal on input pad P. N and a bidirectional pad P. It should be noted that bidirectional pad P. The connections in the circuit of FIG. In the circuit of FIG. The select signal for multiplexer 59 is connected to select line N62484 where, again, "N" is the number that identifies the functional block, B. N, which is to be isolated for testing. The operation of the circuit of FIG. Thus, in ordinary operation of the host chip, signals are directed from circuitry C. Also in the non-test mode of operation, signals are directed from circuitry C. In the test mode, however, signals from circuitry C. In turn, the VDD signal disables pad driver 58 and restricts bidirectional pad P. N is controlled by multiplexer 56 as described in connection with FIG. N to bidirectional pad P. In the circuit, a multiplexer 61 is provided for multiplexing the system signal to pad driver 58 from circuitry C. Also, multiplexer 59 is provided for

multiplexing the enable line for pad driver 58 in the same manner as shown in FIG. It should be noted that select line N62484 is connected to the select inputs of both multiplexers 59 and In the test mode of operation of the circuit of FIG. Instead, the pad driver is enabled by the VSS signal, thereby causing bidirectional pad P. Also during the test mode, multiplexer 61 prevents signals from circuitry C. N are directed to pad P. Further with regard to FIG. In that case, pad driver 58 would be absent and the Z output of multiplexer 61 would be connected directly to pad P. The circuit of FIG. In that case, a circuit such as the one shown in FIG. Also in that case, the instance select lines would be connected to an AND gate which, in turn, would be connected to the select inputs of multiplexers 59 and Thus, pad driver 58 would be enabled concurrently with a test signal output from any one of the functional blocks that are under test. It should be noted that block B. N includes a control port that indicates whether its bidirectional port is in the input or output mode. It should also be noted that two paths must be created to pad P. In the example shown, multiplexer 61 is provided for multiplexing the system signal from circuitry C. Also, multiplexer 59 is interposed between circuitry C. More particularly, multiplexer 59 is connected for multiplexing the enable signal to pad driver 58 with the signal from the control port of functional block B. It should be noted that instance select line N62484 is connected to the select inputs of both multiplexers 59 and As also shown in FIG. In the illustrated embodiment, control unit 73 comprises a multiplexer-like circuit 76 composed of three-state buffers, and an AND gate N and may be connected to the instance select lines N[I] of other functional blocks to be connected to the pad P. When any of the instance select lines N62484 and N[I] is active, the corresponding three-state buffer is enabled, causing the CONTROL signal of the corresponding functional block to either enable or disable the input driver 83 as appropriate. When none of the instance select lines is active the output signal of AND gate 77 causes an additional three-state buffer 76a to disable the input driver N if the bidirectional port is in the output mode. More particularly, when multiple functional blocks each have a bidirectional port that drives the same signal and when all of those ports are connected to a single bidirectional pad P. The inputs of the multiplexer circuit 76 are connected to receive instance select lines corresponding to each of the functional blocks that share the same bidirectional signal and that are being connected to the same pad. Further in that case, AND gate 77 also would receive the same instance select lines. Still further in the case of multiple functional blocks, the inputs of the multiplexer circuit 76 are connected to the control ports of those other functional blocks. Also for employing the circuitry of FIG. And, as mentioned above, the inputs to each multiplexer circuit in each control circuit would include lines from the control ports of all the functional block bidirectional ports that share the same signal and that are to be connected to the bidirectional pad under consideration. It can now be understood that the above-discussed circuits for connection functional block ports to bidirectional pads can be combined. Accordingly, each bidirectional pad of a host chip can have some combination of input, output and bidirectional ports connected to it. An example of such a combination will be provided in conjunction with FIGS. It will be noted that the circuit of FIG. To determine which pad of a host chip should be used to provide an isolation path for testing any one functional block, the following priority method can be employed: For a bidirectional connector on the functional block, choose a pad that has another instance connector connected to the same bidirectional signal mapped to it. That is, try to map all connectors connected to the same bidirectional signal to the same pad. Choose a pad of the same type as an instance connector which already has a signal path added to it. Choose a pad of the same type as the instance connector which does not already have a signal path added to it. Choose a pad of any type which already has a signal path added it. Such a pad will be changed to a bidirectional pad. Choose a pad of any type and, then, change the pad to a bidirectional pad if necessary. Thus, in practice, it is preferred to use chip pads that already have isolation multiplexers added to them. The reason for this is that, once a pad has been disturbed with a multiplexer unit, no additional path delay is incurred by adding more test circuit signals to the pad if the above-described isolation circuits are used. In accordance with the preceding priority method, situations may arise where a host chip has one or more unidirectional input or output pads which must be replaced with bidirectional pads. In practice, the automatic test circuit generation system includes a file with a list of unidirectional pad macro names and a corresponding list of their bidirectional equivalents to provide bidirectional equivalents for the unidirectional pad. Convenient steps for replacing a unidirectional pad with a bidirectional pad are as follows: Disconnect all

signal lines from the unidirectional pad which is to be replaced. The disconnected lines can include ones for the pad signal, an input signal or an output signal, and an optional output enable signal.

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